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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,147	07/16/2003	Robert Ian Gresham	18065	1214

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EXAMINER	
CAVALLARI, DANIEL J	
ART UNIT	PAPER NUMBER
2836	
MAIL DATE	DELIVERY MODE
10/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/621,147	GRESHAM, ROBERT IAN	
	Examiner	Art Unit	
	Daniel J. Cavallari	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-10* is/are pending in the application.

4a) Of the above claim(s) *10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 7/20/2007 have been fully considered but they are not persuasive.

The applicant argues, "The biasing transistors 305 and 306 connect at their bases to each other and to a voltage source. No other connections are made at the bases of the transistors... Rather, any connections between transistors 305 and 306 are made via the collectors of each transistor and additional circuit components..." The Examiner agrees with this analysis of Miki et al. however asserts that the previous rejection based on Miki et al. was properly applied and reads on the applicants claimed invention.

The applicant makes the argument that Miki fails to teach the base of one transistor directly coupled to the base of another transistor without any intervening components but rather the transistors of Miki et al. are coupled through additional circuit components. The Examiner points out that the claim reads "...coupled at its base to a base of at least a second biasing transistor" and fails to see any limitations prohibiting intervening components between the coupling of the transistor bases.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, & 7- 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Miki et al. (US 5,396,131).

In regard to Claims 1 & 9

Miki et al. (hereinafter referred to as Miki)

- A first circuit portion (401) corresponding to a first input port, read on by VA1 & VA2 (Channel 1) (See Figure 10).
- A second circuit portion (402) corresponding to a second input port, read on by the input to transistor gates 301' & 302' (Channel 2) (See Figure 10).
- An output port, read on by I_{10} & I_{20} (See Figure 10).
- Wherein each of the first and second circuit portions includes at least one first transistor, read on by a first differential amplifier (301 and 301') providing a portion of an isolation channel, at least a second transistor, read on by a second differential amplifier (303 and 303') providing a portion of a transmit channel, and two third transistors for providing a control bias which selects an input, read on by 305 & 306 and its equivalent in circuit 402 (See Figure 10) coupled at its base

to a base of a corresponding third transistor (via lines I_{10} & I_{20}) and to control voltage source (309).

In regard to Claim 3

- The third transistors (305, 306, and corresponding transistors for circuit 402) of the first and second portions provides a control bias for selecting which of the first and second input ports are coupled to the output port (I_{10} & I_{20}).

In regard to Claim 4, 7, & 8

- The at least one first transistor (301) comprises two transistors (301 & 302) having emitters coupled to each other and coupled to a collector of the third transistor (305) (See Figure 10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miki et al. and Limberg (US 3,798,376).

Incorporating all arguments above of the switching device taught by Miki, Miki further teaches the use of solid state devices (See Figure 10), but fails to explicitly teach the circuit formed on an integrated circuit.

Limberg teaches solid state components integrated on an integrated circuit (See Column 2, Lines 13-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the switching circuit of Miki into an integrated circuit as taught by Limberg. The motivation would have been the reduced size and weight, increased reliability and economic advantages offered by integrated circuits as opposed to discrete components (See Limberg, column 2, Lines 13-26).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miki et al. and Hester (US 4,460,873).

Incorporating all arguments above of the switching device taught by Miki, Miki teaches amplifiers comprising two transistors but fails to teach them comprising three transistors. Hester teaches the use of amplifiers comprising three transistors in which a Darlington pair (as taught by Miki et al.) is incorporated with two other transistors (96 & 98) in which to create a high gain operational amplifier (See Hester, Figure & Column 4, Lines 25-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the high gain operational amplifier as taught by

Hester with the switch circuit of Miki et al. The motivation would have been to provide a more powerful amplifier capable of outputting better gains.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Cavallari whose telephone number is (571)272-8541. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571)272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel Cavallari

September 20, 2007

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER